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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,815	12/01/2003	Philip George Emma	YOR920030544US1 (163-22)	5561

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,815	EMMA ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-29 and 33-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-29 and 33-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on October 3, 2006.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 33 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 33 and 34 are dependent upon a canceled claim and therefore lack antecedent basis. The claims have been presumed to depend upon claim 22 for purposes of the rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-7, 12-16, 21-26 and 36-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Pomerene et al. (USPN: 4,679,141).

Regarding claims 1-2 and 7, Pomerene discloses a memory storage structure comprising at least one memory storage device (Figure 19, Reference 101; a first meta-structure (branch history table) having a first size and operating at a first speed, which is faster than a second speed for storing meta-information based on information stored in a memory (Figure 19, Reference 131; C 11, L 32-37, L 58-64; C 14, L 67-68; C 15, L 1-3); a second meta-structure hierarchically (branch history table) associated with the first meta-structures, the second meta-structure having a second size larger than the first size and operating at the second speed (Figure 19, Backup area; C 11, L 25-32) such that faster and more accurate prefetching is provided by coaction of the first and second meta-structure (C 16, L 57-60, L 16-68; C 17, entire, C 19, L 6-36; more accurate prefetching [of predicted target addresses] is accomplished by storing predicted target addresses for branches the processor issuing or will use).; a meta-collector (comprised of the analyzer and the stager) configured to collect look ahead context information in the meta-information which includes one of spatial information and temporal state information associated with a memory location, such that the meta-collector provides prefetching (self-loading operations to the active area) to the first meta-structure based upon the look ahead context information (C 17, L 26-67, C 18, entire; C 20, L 46-50).

Regarding claim 3, Pomerene discloses a predicted branch table for identifying a sequence of predicted taken branches that a processor will soon encounter (C 8, L 49-50; C 11, L 58-64; table is comprised of the all the predicted target addresses in the PBHT).

Regarding claims 4-5, Pomerene discloses the meta-information including temporally sequential information and spatially sequential information [defined in specification as branch addresses and predicted target addresses] that are likely to be used in the future (C 8, L 49-50; C 11, L 58-64).

Regarding claim 6, Pomerene discloses the meta-information is correlated to program flow in a processor (the meta-information is branch prediction information which is correlated to the flow of branch instruction in a program and thus is correlated to program flow in a processor).

Regarding claim 12, Pomerene discloses the unique meta-information including at least one of a branch address and a predicted target address for information to be prefetched [from the backup BHT](C 8, L 49-50; C 16, L 51-60).

Regarding claims 13-14, Pomerene discloses a cache (Figure 19, Reference 101); a meta-structure hierarchically arranged on accordance with size and speed such that faster and more accurate prefetching is provided by coaction of hierarchical meta-structures (Figure 19, Reference 131; C 11, L 32-37, L 58-64; Figure 19, Backup area; C 11, L 25-32; C 19, L 6-36; C 16, L 57-60, L 16-68; C 17, entire; more accurate prefetching [of predicted target addresses] is accomplished by storing predicted target addresses for branches the processor issuing or will use); a meta-collector (Figure 19, self loading controls, analyzer and stager) which collects temporally and spatially sequential unique meta-information entries (branch address and predicted target address) corresponding to a cache line to enable hierarchical meta-structure operation to provide prefetching of the meta-information entries to a fastest meta-structure level

based upon look ahead context information (C 16, entire, C 17, entire, C 18, entire, C 19, L 1-36).

Regarding claim 15, Pomerene discloses a predicted branch table for identifying a sequence of predicted taken branches that a processor will soon encounter (C 8, L 49-50; C 11, L 58-64; table is comprised of the all the predicted target addresses in the PBHT).

Regarding claim 16, Pomerene discloses the meta-information is correlated to program flow in a processor (the meta-information is branch prediction information which is correlated to the flow of branch instruction in a program and thus is correlated to program flow in a processor).

Regarding claim 21, Pomerene discloses a plurality of memory storage structures arranged to prefetch information for stages of a circuit (the PBHT prefetches information via the meta-collector from the backup BHT for stages of the branch processing done using the processor and the cache).

Regarding claims 36-48, Pomerene discloses capturing a set of addresses in temporal, the addresses including information associated with each address (Figures 6, 7; BA, TA; C 8, L 22-55); storing sub-sequences of temporal addresses which share spatial context as monolithic entities wherein each monolithic entity is associated with a particular spatial context (C 8, L 22-55; Figures 6-7; Figure 7 illustrates one row of the branch history table which contains sub-sequences of temporal addresses which share spatial context, each pair of BA/TA/V); when a

new spatial context is encountered in the temporal sequence, creating a new monolithic entity associated with the new spatial context, the new spatial context including a temporal sub-sequence of events now associated with the new spatial context (block entry in the PHBT; C 11, L 58-68; C 12, L 1-20).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8-10, 17-20, 22-29 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pomerene (USPN: 4,679,141 in view of Zuraski (USPN: 7,024,545). Regarding claims 8-10 and 17-19, Pomerene discloses the limitations cited above in claims 7 and 13 respectively, however, Pomerene does not explicitly disclose storing the meta-structures in a hierarchically arranged cache including a first level cache and a second level cache. Zuraski discloses storing a meta-structure in a hierarchically arranged cache including a first level cache and a second level cache (C 12, L 61+; C 28, L 57-58; C 14, L 7+; C 12, L 64+; C 28, L 59-60). Pomerene indicates that the PHBT resembles a cache in many ways (C 11, L 38-57) and thus it is evident from one of ordinary skill in the art would consider using a cache since a cache includes faster memory structure. Hence, it would have been obvious to one of ordinary skill in the art to store Pomerene's meta-structure in a hierarchically arranged cache for the desirable purpose of faster system performance.

Regarding claim 20, Pomerene discloses the unique meta-information including at least one of a branch address and a predicted target address for information to be prefetched [from the backup BHT](C 8, L 49-50; C 16, L 51-60).

Regarding claims 22 and 24, Pomerene discloses providing a memory storage structure having a cache (Figure 19, Reference 101), meta-structures hierarchically arranged in accordance with size and speed (Figure 19, Reference 131; C 11, L 32-37, L 58-64; Figure 19, Backup area; C 11, L 25-32; C 19, L 6-36; C 16, L 57-60, L 16-68; C 17, entire) and a meta-collector (Figure 19, self loading controls, analyzer and stager) which collects one of temporally and spatially sequentially unique meta-information entries corresponding to a cache line (C 16, entire, C 17, entire, C 18, entire, C 19, L 1-36); and prefetching meta-information for storage in the meta-structures such that improved speed is provided by coaction of hierarchical meta-structures (C 20, L 1-12, L 54-59); updating meta-information between levels of the hierarchical meta-structures (C 20, L 46-50). Pomerene does not explicitly disclose storing the meta-structures in a hierarchically arranged cache including a first level cache and a second level cache and thus does not disclose updating between the cache and a branch history table and between a first and second level cache. Zuraski discloses storing a meta-structure in a hierarchically arranged cache including a first level cache and a second level cache (C 12, L 61+; C 28, L 57-58; C 14, L 7+; C 12, L 64+; C 28, L 59-60). Pomerene indicates that the PHBT resembles a cache in many ways (C 11, L 38-57) and thus it is evident that one of ordinary skill in the art would consider using caches to store the meta-structures since a cache includes faster memory structure. Modifying

Pomerene's system to incorporate caches to store the meta-structures would provide for updating between the caches and the branch history table. The cached first and second meta-structures comprise the branch history table and thus updating the cache meta-structures provides an update between the cache and the branch history table. Hence, it would have been obvious to one of ordinary skill in the art to store Pomerene's meta-structure in a hierarchically arranged cache for the desirable purpose of faster system performance and to update them as stated above for the desirable purpose of improved performance.

Regarding claim 23, Pomerene discloses the prefetching step including associating cache lines with information addresses in the meta-collector (C 17, L 32-68; C 18, entire; C 19, L 1-35; branch addresses accessed in the cache which are being analyzed by the meta-collector [analyzer/stager])

Regarding claim 25, Pomerene discloses identifying a sequence of predicted taken branches that a processor will soon encounter by employing a predicted branch table (C 8, L 49-50; C 11, L 58-64; table is comprised of the all the predicted target addresses in the PBHT).

Regarding claim 26, Pomerene discloses correlating the meta-information to program flow in the processor (the meta-information is branch prediction information which is correlated to the flow of branch instruction in a program and thus is correlated to program flow in a processor).

Regarding claim 27, Pomerene discloses evicting cache line information from the meta-collector when a corresponding cache line is replaced (inherent, when information is removed/evicted from the meta-structures the information is no longer available for the meta-collector when processing the segment entries to perform prefetching).

Regarding claim 28, Pomerene discloses the limitation cited above for claim 22, however, Pomerene does not disclose storing evicted information to a next level memory in a cache hierarchy. Zuraski discloses storing evicted information to a next level memory in a cache hierarchy (abstract). In Pomerene's system all the data stored in the lower level memory is also stored in the higher level memory and thus when data is evicted there is no need to store the data in the higher level memory. This feature causes the higher level memory to be extremely slow and large. The feature taught by Zuraski provides a fast and efficient method of operating hierarchical memories using smaller hierarchical memories. Hence, it would have been obvious to one of ordinary skill in the art to incorporate Zuraski's teachings with the system taught by Pomerene for the desirable purpose of efficiency and improved performance.

Regarding claim 29, Pomerene discloses the limitations cited above for claim 22, however, Pomerene does not disclose writing to a next level memory area in a cache hierarchy a cache miss address. It is well known in the art to write to a L2 cache to the location, which caused a miss in the L1 cache when using hierarchical caches. This feature provides improved performance by carrying out the memory operation using the cache memories in oppose to writing to main memory. Hence, it would have been obvious to one of ordinary skill in the art to

use hierarchical caches in Pomerene's system such that a cache miss address is written to a higher level cache when a cache miss occurs in the lower level cache for the desirable purpose of improved performance.

Regarding claims 33-34, Pomerene discloses updating meta-information between levels of the hierarchical meta-structure (C 19, L 65-68).

Regarding claim 35, Pomerene disclose (C 12, L 4-8; C 13, L 8-24).

Response to Arguments

8. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Additionally, since the Examiner has revoked the indication of allowable matter which the Applicant has amended the claim to reflect, the Examiner has made this Office Action Non-Final.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Primary Examiner
Art Unit 2187

KNM

December 26, 2006